HN

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/586,868	06/05/2000	Gordon Caruk	0100.0000430	7484

23418 7590 01/03/2005

VEDDER PRICE KAUFMAN & KAMMHOLZ
222 N. LASALLE STREET
CHICAGO, IL 60601

EXAMINER	
KING, JUSTIN	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 01/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/586,868	CARUK ET AL.	
	Examiner	Art Unit	
	Justin I. King	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/14/04* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *40* is/are allowed.

6)☒ Claim(s) *1-6,13,15,18-39 and 41-43* is/are rejected.

7)☒ Claim(s) *7-12, 14, 16-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 21-23 and 25-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Melo et al. (U.S. Patent No 6,040,845).

Referring to claim 21: Melo discloses an internal circuit (figure 1, structure 12) receiving a bus bridge signal from an internal circuit (figure 1, structures 14 and 28), and arbitrating and controlling the signals from any external circuit (figure 1, structures 32a and 302b) from reaching the internal circuit; thus, Melo's internal I/O circuit preventing signals from any external circuit from reaching the internal circuit. Hence, claim is anticipated by Melo.

Referring to claim 22: Melo discloses that the external circuit (figure 2, structure 46) receives the bus bridge signal from the internal bus bridge; and the external circuit reflects the bus bridge signal to the internal I/O circuit (figure 2, structure 40).

Referring to claim 23: Melo discloses that the bus bridge has to arbitrate between the graphic signals and the peripheral master signals; thus, the signals been arbitrated and selected is the internal circuit signal, and therefore the bus receives an internal circuit signal from the

internal circuit and selects one of the internal circuit signal and the external circuit. Melo further discloses that the internal I/O circuit receives an external circuit signal from the external circuit (AGP), and the bus bridge also receives the external circuit signal once the arbiter receives and selects the signals.

Referring to claim 25: Melo's internal circuit does not disclose input buffer.

Referring to claim 26: Melo discloses the PCI bus/protocol.

Referring to claim 27: Melo discloses the AGP bus/protocol.

3. Claims 21-23, 25-27, 29-33, and 35-38 are rejected under 35 U.S.C. 102(e) as being anticipated by Brickford et al. (U.S. Patent No. 6,141,021).

Referring to claim 21: Brickford discloses an internal circuit (figure 1, structure 118) receiving a bus bridge signal from an internal bus bridge (figure 3, combined structures of 114, 124, and 110), and an internal I/O circuit (figure 1, structure 124) arbitrating and controlling the signals from any external circuit (figure 1, structure 120) from reaching the internal circuit; thus, Brickford's internal I/O circuit preventing signals from any external circuit from reaching the internal circuit. Hence, claim is anticipated by Brickford.

Referring to claim 22: Brickford discloses that the external circuit (figure 3, structure 120) receives the bus bridge signal from the internal bus bridge (figure 3, structure 114); and the external circuit reflects the bus bridge signal to the internal I/O circuit (figure 3, structure 124).

Referring to claim 23: Brickford discloses that the bus bridge receiving an internal circuit signal from the internal circuit and an external circuit signal, and selecting one of the internal

circuit signal and the external circuit signal; the internal I/O circuit receiving an external circuit signal from the external circuit (figure 3).

Referring to claim 25: Claim 25 is rejected over Brickford as stated above; furthermore, Brickford does not disclose any input buffer.

Referring to claim 26: Brickford discloses a PCI bus protocol (figures 1 and 2).

Referring to claim 27: Brickford discloses an AGP bus protocol (figure 3).

Referring to claim 29: Brickford discloses a computer system including a processing unit coupled to a processor bus, a memory unit coupled to a memory bus (figures 1 and 2), an integrated bus bridge graphics unit (figure 3, combined structures of 114, 124, and 110), coupled to the memory bus and further operably coupled to provide a signal to an external graphic bus (figure 3, the path between structure 122 and the combined structures of 114, 124, and 110), and an internal circuit (figure 3, structure 118) operably configured to avoid signals from the external graphics bus.

Referring to claim 30: Brickford discloses that the integrated bus bridge graphics unit is further operably coupled to receive a signal from the external graphics bus via an internal I/O circuit (figure 3, structure 124).

Referring to claims 31-33: Brickford's internal I/O circuit is to select the graphic signal communication from either one of the internal circuit or external circuit. Thus, Brickford discloses that the integrated bus bridge unit is further configurable to select and to provide a signal to one of the internal circuit and the external graphics bus, and is further operably configured to isolate the internal circuit from an external graphic bus signal (figure 3).

Referring to claim 35: Brickford does not disclose any input buffer.

Referring to claim 36: It is the communication's purpose to provide signals uncorrupted by transmission line effects.

Referring to claim 37: Brickford discloses a PCI bus protocol (figures 1 and 2).

Referring to claim 38: Brickford discloses an AGP bus protocol (figure 3).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lane et al. (U.S. Patent No. 5,621,900) in view of Kubota (U.S. Patent No. 5,633,599) or Chen et al. (U.S. Patent No. 5,850,530).

Referring to claim 1: Lane discloses a first internal circuit (figure 1, structure 104) to provide a first internal signal via a first internal signal path (figure 1, structure 101), and a selector circuit (figure 1, structure 107) coupled to the first internal circuit via the first internal

signal path, the selector circuit operable to select either the first internal signal or the first external signal. Lane does not explicitly disclose an input buffer for the bridge. Kubota discloses a circuit design with a buffer controlled by a selector (figure 4A). Kubota teaches one to lower down the cost of an integrated circuit by sharing common component/buffer among multiple requests. Chen discloses that it is known to equip the input buffer in the bridge (figures 1-2). Chen discloses that it is known to equip the input buffer to reduce the RETRY signal (columns 1-2).

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Kubota's teaching and the input buffer onto Lane because Kubota teaches one to enhance the bridge's functionality and performance by I/O buffers, and to adapt Chen's bridge input buffer onto Lane because it can reduce the number of RETRY control signals, which will reduce the number of the arbitration attempts.

7. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable by Melo in view of Kubota or Chen.

Referring to claim 1: Melo discloses a first internal circuit (figure 1, structure 12) operable to provide a first internal signal via a first internal signal path (figure 1, structure CPU bus), a selector circuit (figure 1, structure 14) coupled to the first internal circuit via the first internal signal path, and the input buffer, the selector circuit operable to select either the first internal signal or the first external signal. Melo does not explicitly disclose an input buffer. Kubota discloses a circuit design with a buffer controlled by a selector (figure 4A). Chen

discloses that it is known to equip the input buffer in the bridge (figures 1-2). Chen discloses that it is known to equip the input buffer to reduce the RETRY signal (columns 1-2).

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Kubota's teaching and the input buffer onto Melo because Kubota teaches one to enhance the bridge's functionality and performance by I/O buffers and to adapt Chen's bridge input buffer onto Melo because it can reduce the number of RETRY control signals, which will reduce the number of the arbitration attempts.

8. Claims 1-5, 13, 15, 18-20, 24, 34, 41-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brickford in view of Kubota or Chen.

Referring to claim 1: Brickford discloses a first internal circuit (figure 3, structure 118) operable to provide a first internal signal via a first internal signal path (figure 3, path between the structure 118 and the combined structures of 124, 110, and 114), receiving a first external signal via a first external signal path (figure 3, path between the structure 122 and the combined structures of 124, 110, and 114), a selector circuit (figure 3, structure 124) coupled to the first internal circuit via the first internal path, and to select either the first internal signal or the first external signal.

Brickford does not explicitly disclose an input buffer, but the I/O buffer is a well-known practice in the computer art; furthermore, Kubota discloses a circuit design with a buffer controlled by a selector (figure 4A). Chen discloses that it is known to equip the input buffer in the bridge (figures 1-2). Chen discloses that it is known to equip the input buffer to reduce the RETRY signal (columns 1-2). Hence, it would have been obvious to one having ordinary skill in

the computer art at the time Applicant made the invention to adapt Kubota's teaching and the input buffer onto Brickford because Kubota teaches one to enhance the bridge's functionality and performance by I/O buffers, and to adapt Chen's bridge input buffer onto Brickford because it can reduce the number of RETRY control signals, which will reduce the number of the arbitration attempts.

Referring to claim 2: Brickford discloses an output buffer (figure 6, structure 170) to receive a second internal signal (the signal from the AGP controller) and to provide the signal via the first external signal path (figure 3, structure 110). The path conveys the data into the buffer is the claimed second internal signal path. Although Brickford does not explicitly and clearly label a separate second internal signal path and the first internal signal path for conveying signals into the output buffer, the court has held that duplication of the working parts of a device and forming in one piece an article which has formerly been formed in two pieces involve only routine skill in the art (St. Regis Paper Co. v. Bemis Co., 193 USPQ 8 and Howarde v. Detroit Stove Works, 150 U.S. 164). Such that it only takes routine skill in the computer art to add an additional internal signal path and to integrate the external output path and external input path into one external path.

Referring to claim 3: Claim 3 is rejected over Brickford as stated above; furthermore, the Brickford's system is inherently operable to propagate graphic signal with a common protocol.

Referring to claim 4: Claim 4 is rejected over Brickford as stated above; furthermore, Brickford discloses a PCI bus protocol (figures 1 and 2).

Referring to claim 5: Claim 5 is rejected over Brickford as stated above; furthermore, Brickford discloses an AGP bus protocol (figure 3).

Referring to claim 13: Claim 13 is rejected over Brickford as stated above; furthermore, the circuit is inherent to have a bus interface since it has to connect to a bus for conveying graphic signals.

Referring to claim 15: Claim 15 is rejected over Brickford as the argument for claim 2 stated above.

Referring to claim 18: It is the communication's purpose to provide signals uncorrupted by transmission line effects.

Referring to claim 19: Claim 19 is rejected over Brickford as stated above; furthermore, since the input buffer is meant to convey the signals to the AGP controller rather to the on-chip graphic circuit, it is said that since the input buffer is inoperable to provide the external signal from the external circuit to the first internal circuit.

Referring to claim 20: Claim 20 is rejected over Brickford as the argument for claim 19 stated above; furthermore, the output buffer is an internal buffer designed for conveying the internal signal to the external circuit, therefore, it is said that the output buffer is inoperable to provide the first external signal from the first external signal path to the first internal circuit.

Referring to claim 24: Claim 24 is rejected over Brickford as stated above; furthermore, although Brickford does not explicitly disclose multiplexing as the selecting mean, the multiplexing is a well-known selecting practice in the computer art, and Applicant didn't challenge the well-known knowledge of the multiplexer.

Referring to claim 34: Brickford discloses that the integrated bus bridge isolates the external signal from the internal circuit (figure 1), but Brickford does not explicitly disclose an input buffer for receiving the external signal. Kubota discloses a circuit design with a buffer

controlled by a selector (figure 4A). Chen discloses that it is known to equip the input buffer in the bridge (figures 1-2). Chen discloses that it is known to equip the input buffer to reduce the RETRY signal (columns 1-2). Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Kubota's teaching and the input buffer onto Brickford because Kubota teaches one to enhance the bridge's functionality and performance by I/O buffers, and to adapt Chen's bridge input buffer onto Brickford because it can reduce the number of RETRY control signals, which will reduce the number of the arbitration attempts.

9. Claims 6, 28, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brickford in view of Applicant's admitted prior art the NGP protocol or Colton et al. (U.S. Patent No. 4,529,840): Brickford does not disclose the NGP protocol. Both Applicant's disclosed prior art and Colton disclose that the NGP is a well-known industrial practice as an alternative to AGP and PCI at the time applicant made the invention. Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt NGP onto Brickford because NGP is a known alternative to the AGP and PCI in designing the computer structure.

Allowable Subject Matter

10. Claim 40 is allowed.

11. Claims 7-12, 14, 16-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter:

Referring to claim 7: A configurable AGP interface circuit as structurally illustrated in figures 4 and 5 is structured to include a dedicated output buffer for outputting the internal signal to the add-in AGP card and this internal output signal does not go through the select circuit. The circuit is constructed in the structuring arrangement as the followings; a first internal circuit operable to provide a first internal signal via a first internal signal path; an input buffer operable to receive a first external signal via an first external signal path; and a selector circuit coupled to the first internal circuit via the first internal signal path, and to the input buffer, the selector circuit operable to select either the first internal signal or the first external signal to provide a selected signal; and an output buffer operative to receive a second internal signal via a second internal signal path and to provide the second internal signal via the first external signal path; and a second internal circuit operable to provide the second internal signal via the second internal signal path and to receive the selected signal via a third internal signal path, the selector circuit inoperable to receive the second internal signal; and the second internal circuit is operable to provide the second internal signal via the second internal signal path to both the first internal circuit and the output buffer.

Referring to claims 8-12 and 14: Claims are allowed because they incorporate the allowable subject matter from claim 7.

Referring to claim 16: A configurable AGP interface circuit as structurally illustrated in figures 4 and 5 is structured to include a dedicated output buffer for outputting the internal signal to the add-in AGP card and this internal output signal does not go through the select circuit. The circuit is constructed in the structuring arrangement as the followings; a configurable interface circuit comprising: a first internal circuit operable to provide a first internal signal via a first internal signal path; an input buffer operable to receive a first external signal via an first external signal path; and a selector circuit coupled to the first internal circuit via the first internal signal path, and to the input buffer, the selector circuit operable to select either the first internal signal or the first external signal to provide a selected signal; a bus bridge, comprising a bus interface, operable to provide a second internal signal to the first internal circuit via a second internal signal path and to receive the selected signal via a third internal signal path, and an output buffer operative to receive the second internal signal via the second internal signal path and to provide the second internal signal via the first external signal path such that the input buffer and the selector circuit are inoperable to receive the second internal signal.

Referring to claim 17: Claim is allowed because it incorporates the allowable subject matter from claim 16.

Referring to claim 40: A configurable AGP interface circuit as structurally illustrated in figures 4 and 5 is structured to include a dedicated output buffer for outputting the internal signal to the add-in AGP card and this internal output signal does not go through the select circuit. The circuit is constructed in the structuring arrangement as the followings; an internal graphics controller operable to provide a first internal signal via a first internal signal path; an input buffer operable to receive a first external signal via an first external signal path; a selector circuit

coupled to the internal graphics controller via the first internal sigh path and to the input buffer, the selector circuit operable to select either the first internal signal or the first external signal to provide a selected signal; a bus bridge comprising a bus interface operable to provide a second internal signal to the internal graphics controller via a second internal signal path and to receive the selected signal via a third internal signal path; and an output buffer operative to receive the second internal signal via the second internal signal path and to provide the second internal signal via the first external signal path such that the input buffer and the selector circuit are inoperable to receive the second internal signal.

Response to Arguments

13. In response to Applicant's argument that the prior art Melo arbitrates the AGP instead of peripherals (Remark, page 9, paragraph 2, lines 4-6): The Office Action recites the structure 28, the south bridge, for arbitrating the peripherals, structures 23a and 302b. The AGP arbitration as stated in the Melo's abstract is handled by the structure 14, the north bridge.

14. In response to Applicant's argument that Melo's suspended pipeline processing does not prevent the singles from reaching the internal circuit (Remark, page 9, paragraph 2, last 4 lines, page 10, paragraph 2, lines 3-4): The claim is interpreted as board as possible during prosecution. The claimed limitation is not construed as to preclude the interpretation of the suspended pipeline processing.

15. In response to Applicant's argument that the internal circuit does not arbitrate the graphic master structure 46 (Remark, page 10, paragraph 3, lines 5-6): The internal circuit is the internal bridge (figure 1, structures 14 and 28), which arbitrates the graphic masters and the peripherals.

16. In response to Applicant's argument that Brickford fails to anticipate claim 21 (Remark, page 11, paragraph 1): Applicant merely alleges that Brickford fails to anticipate the claim, but does not provide the reason why the Office Action's Rejection is incorrect. Brickford discloses an internal circuit (figure 1, structure 118) receiving a bus bridge signal from an internal bus bridge (figure 3, combined structures of 114, 124, and 110), and an internal I/O circuit (figure 1, structure 124) arbitrating and controlling the signals from any external circuit (figure 1, structure 120) from reaching the internal circuit; thus, Brickford's internal I/O circuit preventing signals from any external circuit from reaching the internal circuit. Hence, claim is anticipated by Brickford.

17. In response to Applicant's argument that Brickford does not teach the external bus (Remark, page 11, paragraph 4, lines 5-7): As stated in the Rejection above, Brickford discloses the external graphic bus (figure 3, the path between structures 122, 114, 124, and 110). Whether this is an internal bus or an external bus is subjected to one's opinion and interpretation, which is not explicitly construed or defined within the scope of the claimed limitations, and the claim is interpreted as board as possible during prosecution.

18. In response to Applicant's argument that the Office Action fails to show how the selector circuit equated to host bus bridge 107 (Remark, page 11, last line): As one with ordinary skill in the computer art will know the operations of a bridge, which is to arbitrate and to forward the signals between two buses. The arbitrating and forwarding means are the selecting means. Hence, the bridge is equivalent to the claimed selector circuit.

19. In response to Applicant's argument that the prior arts do not explicitly state the suffering "retry" problem or input buffer (Remark, page 12, paragraph 1, line 5, paragraph 2, line

3): Although the prior arts Lane and Melo do not explicitly state the suffering of "retry" problem or input buffer, it is not required for the prior art to stated the needs of teachings from the secondary art. The Office Action provides additional references to show that both the "retry" and input buffer are conventional practices, and there are novelty in employing "retry" and input buffer in a bridge. In fact, as Applicant may also be aware, the "Retry" is a part of PCI standard.

20. In response to Applicant's argument that Melo does not teach a selector circuit (Remark, page 12, paragraph 2,m lines 5-6): As Applicant stated, Melo teaches the arbitration, which is equivalent to the claimed selector circuit.

21. In response to Applicant's argument that Brickford fails to describe the output buffer as operative to receive a second internal signal via the second internal path and to provide the internal signal via the first external signal path (Remark, page 13, paragraph 2, lines 1-2): Brickford discloses an output buffer (figure 6, structure 170) to receive a second internal signal (the signal from the AGP controller) and to provide the signal via the first external signal path (figure 3, structure 110). The path conveys the data into the buffer is the claimed second internal signal path. Although Brickford does not explicitly and clearly label a separate second internal signal path and the first internal signal path for conveying signals into the output buffer, the court has held that duplication of the working parts of a device and forming in one piece an article which has formerly been formed in two pieces involve only routine skill in the art (St. Regis Paper Co. v. Bemis Co., 193 USPQ 8 and Howarde v. Detroit Stove Works, 150 U.S. 164). Such that it only takes routine skill in the computer art to add an additional internal signal path and to integrate the external output path and external input path into one external path.

22. In response to applicant's argument that there is no suggestion to combine the references (Remark, page 13, paragraph 2, lines 8-9): The examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Chen teaches one to reduce the retry signal by employing an input buffer (columns 1-2) and Kubota teaches one to lower down the cost of the integrated circuit by employing a selector to share a common component among multiple requests.

Conclusion

23. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin I. King whose telephone number is 571-272-3628. The examiner can normally be reached on Monday through Friday, 9:00 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Justin King
December 22, 2004

SUMATI LEFKOWITZ
PRIMARY EXAMINER